New Simple CMOS Realization of Voltage Differencing Transconductance Amplifier and Its RF Filter Application

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Abstract. *The voltage differencing transconductance amplifier (VDTA) is a recently introduced active element for analog signal processing. However, the realization of VDTA is not given by any author yet. In this work, a new and simple CMOS realization of VDTA is presented. The proposed block has two voltage inputs and two kinds of current output, so it is functional for voltage- and transconductance-mode operation. Furthermore, VDTA exhibits two different values of transconductance so that there is no need to external resistors for VDTA based applications which seems to be a good advantage for analog circuit designer. A CMOS implementation of VDTA and a voltage-mode VDTA based filter are proposed and simulated. An application example of fourth order flat-band band-pass amplifier is given and the performance of the circuit is demonstrated by comparing the theory and simulation.*

Keywords

Voltage differencing transconductance amplifier, voltage mode filter, CMOS integrated circuit.

1. Introduction

Active elements are widely used in analog signal progressing, such as filters, oscillators and inductance simulators etc. Many active elements were and are being proposed [1] – [13] because there are important features relative to each other, such as input and/or output terminal can be different/same features, any parameter can be controlled by external voltage or current etc. New designs are provided for researchers with these new proposed active elements. In [14] the present-day active elements are reviewed and several new elements are introduced. However, the realizations of the newly introduced active elements are not given. One of these active elements is VDTA, which can be compared with CDTA, a previously introduced active element [9]. In CDTA, differential input current (I_p, I_n) flows over the Z terminal. The voltage drop at the terminal Z is transferred to current at the terminal X by a transconductance gain. Several CDTA applications are given in the literature [15] – [20].

In VDTA, differential input voltage (V_{VP} ,V_{VN}) is transferred to current at the terminal Z by first transconductance gain and the voltage drop at the terminal Z is transferred to current at the terminals X+ and X- (negative of X+) by second transconductance gain. Both transconductance are electronically controllable by external bias currents. Compared to other active blocks [1] – [8], the advantageous feature of VDTA is that this new element exhibits two different values of transconductances so that several applications such as biquad filters, oscillator, inductance and FDNR (frequency dependent negative resistor) simulator can be realized with a single active block employing one or two capacitors. Another important feature, this block can be used easily at transconductance mode applications owing to input terminals is voltage and output terminals is current.

In this paper, a new CMOS implementation of VDTA is given. The performance of the proposed circuit is tested with an application example of voltage-mode filter. By selecting input terminal voltages, this construction can generate the standard filter functions for voltage-mode. The proposed circuit employing minimum number of passive and active components uses no external resistors. Furthermore, no parameter matching condition is required.

2. Circuit Description

The circuit symbol of the proposed active element, VDTA, is shown in Fig. 1, where *V*P and *V*N are input terminals and Z, X+ and X- are output terminals. All terminals exhibit high impedance values. Using standard notation, the terminals relationship of an ideal VDTA can be characterized by:

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_Z \end{bmatrix}. \quad (1)$$

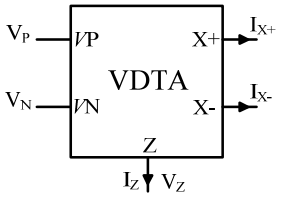

Fig. 1. The circuit symbol of the VDTA.

Consequently, the above describing-equations, the input stage and output stage can be simply implemented by floating current sources. According to input terminals, an output current at Z terminal is generated. The intermediate voltage of Z terminal is converted to output currents. The new CMOS realization of the VDTA is shown in Fig. 2. The introduced circuit employs two Arbel-Goldminz transconductances [21]. Input and output transconductance parameters of VDTA element in the circuit are determined by the transconductance of outputs transistors. It can be approximated as

$$g_{m1} = (g_3 + g_4)/2\,, \tag{2a}$$

$$g_{m2} = (g_5 + g_8)/2 \quad \text{or} \quad g_{m2} = (g_6 + g_7)/2 \tag{2b}$$

where g_i is the transconductance value of i^{th} transistor defined by

$$g_i = \sqrt{I_{Bi}.\mu_i.C_{OX}\left[\frac{W}{L}\right]_i}\,,$$

μ_i is (i = n, p) the mobility of the carrier for NMOS (n) and PMOS (p) transistors, C_{OX} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length and I_{Bi} is bias current of i^{th} transistor.

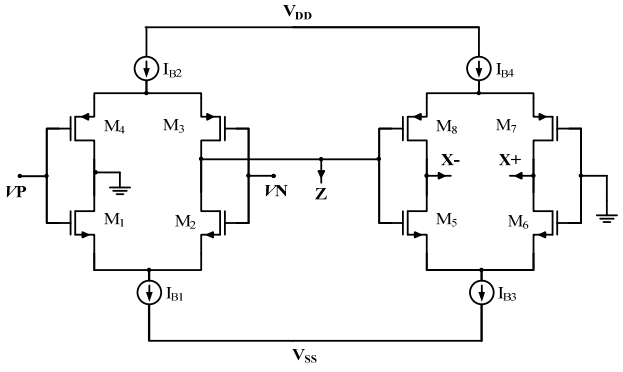

Fig. 2. CMOS implementation of VDTA.

3. Application Examples

The VDTA is very flexible in different mode filter realizations. The advantages obtained are that the values of transconductances are adjusted by bias currents to realize these circuits without any requirement of external resistors.

The realization of voltage-mode filter with dual-inputs dual-outputs is shown in Fig. 3. This proposed circuit employing a single VDTA and only two capacitors realizes LP, BP and HP filter. Circuit analysis yields voltage-mode biquad transfer functions shown in (3) – (6).

If $V_1 = V_{IN}$ and $V_2 = 0$, then

$$BP \rightarrow \frac{V_{OUT1}}{V_{IN}} = \frac{sC_1 g_{m1}}{s^2 C_1 C_{2T} + sC_1 g_{m2} + g_{m1} g_{m2}}\,, \tag{3}$$

$$LP \rightarrow \frac{V_{OUT2}}{V_{IN}} = \frac{g_{m1} g_{m2}}{s^2 C_1 C_{2T} + sC_1 g_{m2} + g_{m1} g_{m2}}\,. \tag{4}$$

If $V_2 = V_{IN}$ and $V_1 = 0$, then

$$HP \rightarrow \frac{V_{OUT1}}{V_{IN}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_{2T} + sC_1 g_{m2} + g_{m1} g_{m2}}\,, \tag{5}$$

$$BP \rightarrow \frac{V_{OUT2}}{V_{IN}} = \frac{sC_2 g_{m2}}{s^2 C_1 C_{2T} + sC_1 g_{m2} + g_{m1} g_{m2}}\,. \tag{6}$$

The natural frequency ω_0 and quality factor Q can be given as follows;

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_{2T}}}\,, \tag{7}$$

$$Q = \sqrt{\frac{C_{2T} g_{m1}}{C_1 g_{m2}}}\,. \tag{8}$$

The passive sensitivities of natural frequency and quality factor for the proposed circuit of Fig. 3 are given as;

$$S^{\omega_0}_{g_{m1}} = S^{\omega_0}_{g_{m2}} = -S^{\omega_0}_{C_1} = -S^{\omega_0}_{C_{2T}} = \frac{1}{2}\,, \tag{9}$$

$$S^{Q}_{g_{m1}} = -S^{Q}_{g_{m2}} = S^{Q}_{C_{2T}} = -S^{Q}_{C_1} = \frac{1}{2}\,. \tag{10}$$

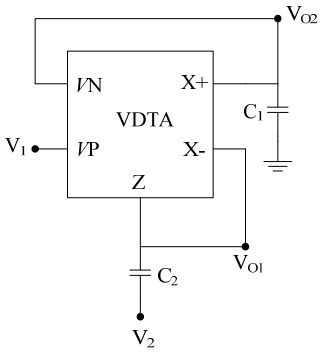

Fig. 3. Application of proposed VDTA.

The non-ideal effects of the CMOS VDTA include input parasitic capacitances and output parasitic conductances. Parasitic capacitances (C_P) appear parallel at VP, VN and Z terminals, while parasitic conductances (G_P) appear parallel at Z, X+ and X- terminals. The parasitic impedances belong to VDTA based filter are indicated in Fig. 4.

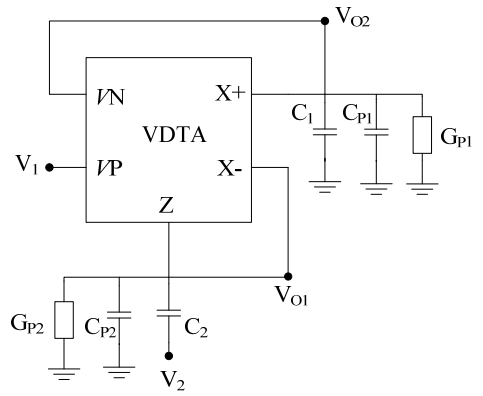

Fig. 4. Parasitic impedances of VDTA affecting filter operation.

Considering the above parasitic impedances, the transfer functions analyses lead to the following result:

If $V_1 = V_{IN}$ and $V_2 = 0$, then

$$BP \rightarrow \frac{V_{OUT1}}{V_{IN}} = \frac{s g_{m1}\left(C_1 + C_{P1}\right) + g_{m1} G_{P1}}{\Delta s}, \tag{11}$$

$$LP \rightarrow \frac{V_{OUT2}}{V_{IN}} = \frac{g_{m1} g_{m2}}{\Delta s}. \tag{12}$$

If $V_2 = V_{IN}$ and $V_1 = 0$, then

$$HP \rightarrow \frac{V_{OUT1}}{V_{IN}} = \frac{s^2 C_2\left(C_1 + C_{P1}\right) + s C_2 G_{P1}}{\Delta s}, \tag{13}$$

$$BP \rightarrow \frac{V_{OUT2}}{V_{IN}} = \frac{s C_2 g_{m2}}{\Delta s} \tag{14}$$

where Δs is the characteristic equation and is given by

$$\begin{aligned} \Delta s = {} & s^2\left(C_1 + C_{P1}\right)\left(C_2 + C_{P2}\right) \\ & + s\left(\left(C_2 + C_{P2}\right) G_{P1} + \left(C_1 + C_{P1}\right)\left(g_{m2} + G_{P2}\right)\right) \\ & + g_{m1} g_{m2} + G_{P1}\left(g_{m2} + G_{P2}\right) \end{aligned} \tag{15}$$

where $C_{P1} = C_{PVN}$, $C_{P2} = C_{PZ}$, $G_{P1} = G_{PX+}$ and $G_{P2} = G_{PZ} + G_{PX-}$ are consisted of parasitic impedances. The parameter natural frequency ω_0 and quality factor Q of the filter with effects of parasitic impedances are calculated as

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2} + G_{P1}\left(g_{m2} + G_{P2}\right)}{\left(C_1 + C_{P1}\right)\left(C_2 + C_{P2}\right)}}, \tag{16}$$

$$Q = \frac{\sqrt{\left(C_1 + C_{P1}\right)\left(C_2 + C_{P2}\right)}\sqrt{g_{m1} g_{m2} + G_{P1}\left(g_{m2} + G_{P2}\right)}}{\left(C_2 + C_{P2}\right) G_{P1} + \left(C_1 + C_{P1}\right)\left(g_{m2} + G_{P2}\right)}. \tag{17}$$

It is observed from equations (16) and (17) that parasitic capacitances and conductances increase effective capacitances and conductances respectively so values of ω_0 and Q decrease. It should be mentioned that some parameters such as output conductances at Z, X+ and X- terminals of the VDTA can be improved by using improved FCS stage [22] in its CMOS structure instead of simple FCS stage. In this way, output parasitic conductances can be easily ignored.

VDTA is a g_m based active element. Therefore, temperature dependence of VDTA is related to temperature dependence of g_m

$$g_m = \mu_n \frac{W}{L} C_{OX}\left(V_{GS} - V_T\right). \tag{18}$$

Depending upon the absolute magnitude of V_T, the approximate absolute change in V_T is –2.4 mV/°C.

The temperature dependence of mobility is

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-1.5}. \tag{19}$$

The threshold voltage decreases with the temperature in order 0.24 %, but the mobility decreases with the temperature in order 1.5 %. Obviously, mobility decreasing is dominant on the g_m and g_m decreases with the increasing temperature.

4. Simulation Results

We perform the simulations by using LTSPICE program with TSMC CMOS 0.18 µm process parameters. The aspect ratios of the transistors are given in Tab. 1. Supply voltages are taken as $V_{DD} = -V_{SS} = 0.9$ V and $I_{B1} = I_{B2} = I_{B3} = I_{B4} = 150\ \mu A$ biasing currents are used. Simulation results show that this choice yields transconductance values of VDTA as $g_{m1} = g_{m2} = 636.3$ µA/V and the parasitic capacitance at the Z terminal is specified as $C_p = 0.15$ pF. The DC transfer characteristic of I_{X+} and I_{X-} against V_Z for output stage of proposed VDTA is shown in Fig. 5. The DC transfer characteristic of input stage of VDTA is the same as I_{X+} of output stage.

Transistors	W(µm)	L(µm)
M_1, M_2, M_5, M_6	3.6	0.36
M_3, M_4, M_7, M_8	16.64	0.36

Tab. 1. Transistors aspect ratios for the VDTA.

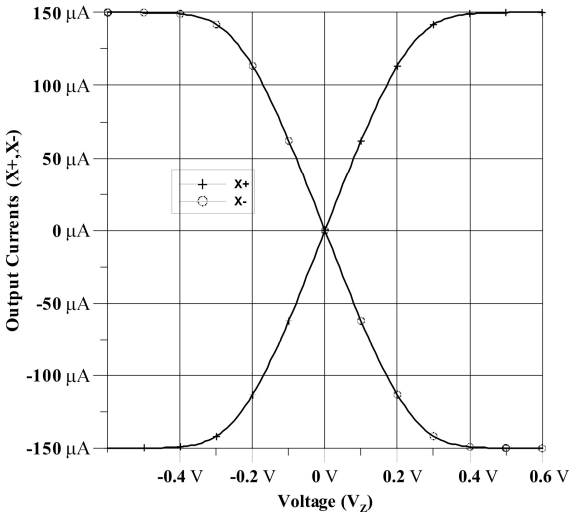

Fig. 5. The DC transfer characteristic of the VDTA.

The proposed circuit in Fig. 3 is simulated with the following passive element values $C_1 = 1.013$ pF and $C_2 = 0.863$ pF, a total capacitance of $C_{2T} = 1.013$pF at Z terminal which results in quality factor of $Q = 1$ and 100 MHz center frequency. Fig. 6 illustrates the simulated results of LP, BP and HP of voltage-mode gain-frequency responses by selecting input voltage terminals.

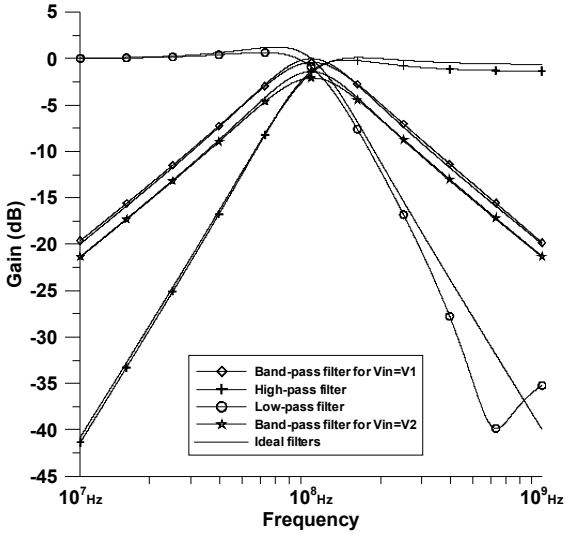

Fig. 6. Gain-frequency responses of voltage-mode LP, BP and HP signals.

Baseband active filters should be low-pass networks for zero IF and band-pass networks for IF or super-heterodyne applications. Fig. 7 shows the block diagram of a typical multi-step superheterodyne receiver with a digital back-end. As the figure shows, a sequence of filter operations is used to convert the desired signal from radio frequency (RF), typically in the VHF (30 MHz to 300 MHz) range, down to one or more intermediate frequencies (IFs) and finally down to baseband, where the signal is digitized by an ADC [23].

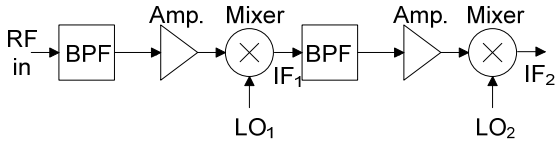

Fig. 7. A typical superheterodyne receiver.

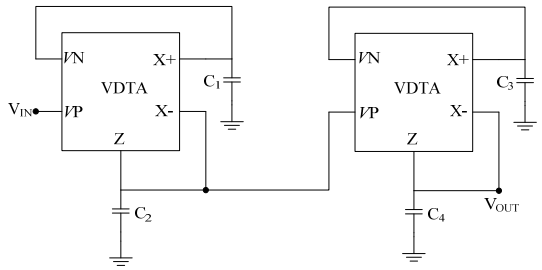

Fig. 8. Double tuned amplifier's realization using the proposed circuit.

For the above typical superheterodyne receiver, a band-pass filter is realized with double tuned amplifiers [24]. Bandwidth $B = \Delta\omega/2\pi$ of this band-pass filter is equal to the diameter of the pole circle. The transfer function of the example application illustrated in Fig. 8 is given by

$$\frac{V_{OUT}}{V_{IN}} = K_0 \frac{\frac{\omega_{p1}}{Q_{p1}} s}{s^2 + \frac{\omega_{p1}}{Q_{p1}} s + \omega_{p1}^2} \cdot \frac{\frac{\omega_{p2}}{Q_{p2}} s}{s^2 + \frac{\omega_{p2}}{Q_{p2}} s + \omega_{p2}^2} \tag{20}$$

where K_0 is the gain factor, ω_{p1}, ω_{p2}, Q_{p1} and Q_{p2} are the pole frequencies and the quality factors of the proposed second order band-pass filter given by (7) – (8), respectively. The pole frequencies are determined to slightly different frequencies, which can be approximated by

$$f_{p1} = \frac{\omega_{p1}}{2\pi} = f_0 + \frac{B}{2}\sin\left(45^\circ\right), \tag{21}$$

$$f_{p2} = \frac{\omega_{p2}}{2\pi} = f_0 - \frac{B}{2}\sin\left(45^\circ\right). \tag{22}$$

To obtain a filter with a center frequency 100 MHz and bandwidth of 80 MHz, the pole frequencies and quality factors of the proposed circuits are chosen as $f_{p1} = 71.716$ MHz, $f_{p2} = 128.284$ MHz and $Q_{p1} = Q_{p2} = 1$, respectively. The transconductance and capacitance values providing these properties are determined as $g_{m1,2,3,4} = 636.3$ μA/V and $C_1 = 0.789$ pF, $C_2 = 0.639$ pF, $C_3 = 1.412$ pF, $C_4 = 1.262$ pF. The frequency responses of the amplifier obtained from theory and from LTSPICE simulation are shown in Fig. 9. The center frequency and the bandwidth of the designed amplifier are determined with LTSPICE simulation as $f_0 = 95.65$ MHz and B = 82.54 MHz respectively.

Dependence of the center frequency of the double tuned amplifier on biasing currents is given in Fig. 10 by changing the biasing currents $I_{B1,2,3,4}$ between 5 and 360 μA. Capacitors with the above values of their capacitances were used.

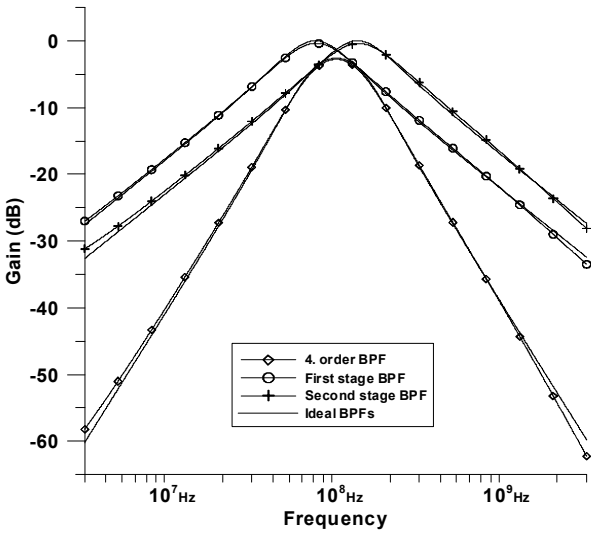

Fig. 9. Ideal and simulation frequency responses of the designed double tuned amplifier.

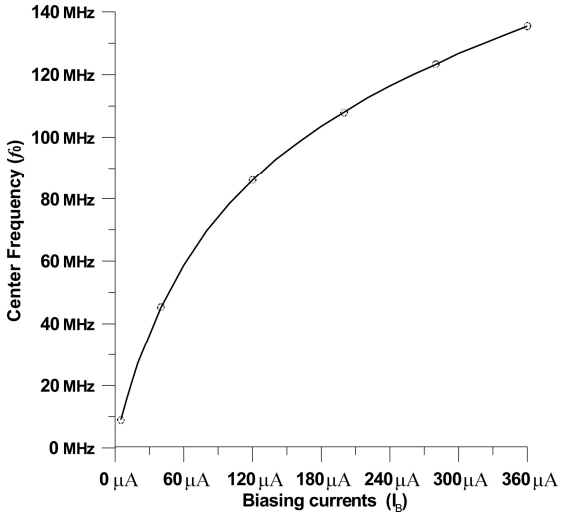

Fig. 10. Dependence of center frequency on biasing currents (I_{Bs}).

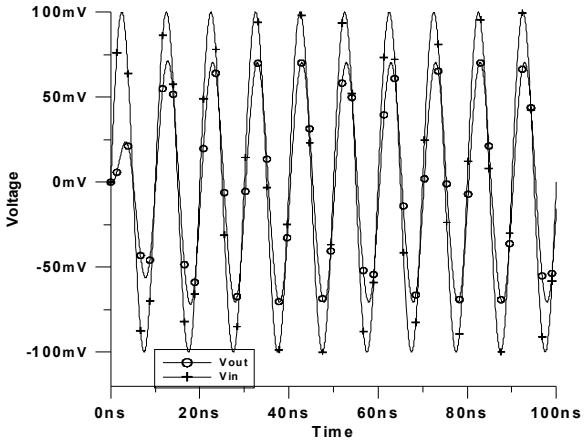

Fig. 11. Time domain response of the circuit in Fig. 3 for 200 mV (p-p) 100 MHz sine wave for voltage-mode band-pass filter configuration.

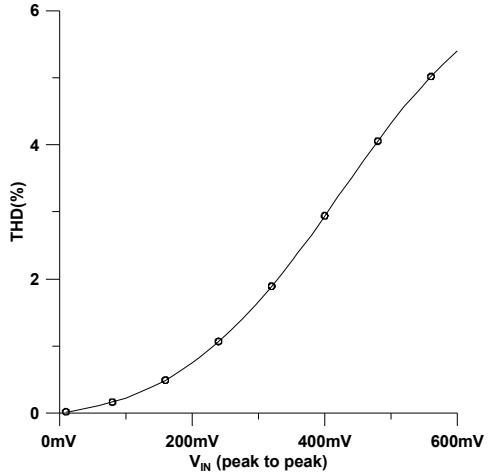

Fig. 12. Dependence of output voltage harmonic distortion on input voltage amplitude of the double toned amplifier.

To test the input dynamic range of the double tuned amplifier, a sinusoidal input signal of $f_0 = 100$ MHz is applied to the input of the band-pass filter and the output waveform is obtained by simulations. Fig. 11 shows that the input dynamic range of the filter response extends up to amplitude of 200 mV (peak to peak) without significant distortion. The THD results for the double tuned amplifier are given in Fig. 12, which clearly shows that for an input signal lower than 500 mV (p-p), the THD remains in acceptable limits i.e. 5 % thus confirming the practical utility of the proposed circuit.

5. Conclusion

A new voltage differencing transconductance amplifier, VDTA is presented. A new and simple CMOS realization of this element is given. In contrary to simple realization topology employing a few numbers of transistors the proposed circuit exhibits good performance. Due to these properties, frequency response of this topology for the VDTA is suitable for high frequency applications. Besides, since supply voltages are ±0.9V, the circuit is suitable for low voltage applications. An application example of a voltage-mode filter employing the proposed CMOS VDTA realization has been presented. In this application of VDTA, disadvantage caused by external resistors was avoided, since the proposed filter is constructed employing only a single active element, VDTA, and two capacitors, where the value of transconductances can be adjusted by biasing currents. Simulation results that are simulated using LTSPICE confirm the theoretical results.

Acknowledgments

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